EAST SEARCH

8/30/05

L#	Hits	Search String	Databases
S1	45055	(microprocessor$1 or processor$1) with performance	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	6030	(computer with program) with performance	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	49753	S1 or S2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	400	(microprocessor$1 or processor$1) with (emulat$3 near2 mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	17039	(microprocessor$1 or processor$1) with ((normal or operat$3) near2 mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	239	S4 and S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	62	S3 and S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	239	S6 or S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	82	S8 and (instruction with counter$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	32	S8 and (cycle with counter$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	210	S8 and (execut$3 with (program or instruction$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	3	S8 and (counter with (threshold or limit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	3	S8 and (counter with (threshold$1 or limit$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	52	S8 and (counter with read$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	90	S8 and (execut$3 with point$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	118	S8 and (execut$3 with (complet$3 or end$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	54	S8 and (execut$3 with speed)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	1	S8 and (execut$3 with assess$4 with point$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	1	S8 and (assess$4 with point$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	106	S8 and ((start$3 or end$3) with (program or point$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	213	S11 or S16 or S20	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	84	S8 and (instruction with cycle$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	74	S8 and (clock with cycle$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	150	S9 or S10 or S12 or S14 or S15 or S17 or S18 or S22 or S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	148	S24 and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	150	S24 or S25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	113	S9 or S10 or S12 or S14 or S22 or S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	213	S11 or S15 or S16 or S17 or S18 or S20	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	111	S27 and S28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	113	S27 or S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	17200	S4 or S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	64508	S3 or S31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	325	S32 and (cycles near2 "per instruction")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	1	S6 and S33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	43	S31 and (cycles near2 "per instruction")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	42	S32 and ((cycles near2 "per instruction") with (calculat$3 or comput$3 or estimat$3 or predict$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S37	45090	(microprocessor$1 or processor$1) with performance	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38	6037	(computer with program) with performance	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	49793	S37 or S38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40	400	(microprocessor$1 or processor$1) with (emulat$3 near2 mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	17046	(microprocessor$1 or processor$1) with ((normal or operat$3) near2 mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	17207	S40 or S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	64553	S39 or S42	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	325	S43 and (cycles near2 "per instruction")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	42	S43 and ((cycles near2 "per instruction") with (calculat$3 or comput$3 or estimat$3 or predict$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	239	S40 and S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	62	S39 and S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	239	S46 or S47	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	82	S48 and (instruction with counter$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	32	S48 and (cycle with counter$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	210	S48 and (execut$3 with (program or instruction$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	3	S48 and (counter with (threshold or limit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	52	S48 and (counter with read$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	90	S48 and (execut$3 with point$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	118	S48 and (execut$3 with (complet$3 or end$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	54	S48 and (execut$3 with speed)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	1	S48 and (execut$3 with assess$4 with point$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	106	S48 and ((start$3 or end$3) with (program or point$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	84	S48 and (instruction with cycle$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	74	S48 and (clock with cycle$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S61	113	S49 or S50 or S52 or S53 or S59 or S60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	213	S51 or S54 or S55 or S56 or S57 or S58	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	111	S61 and S62	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	113	S61 or S63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S65	16	S44 and (emulat$3 near2 mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S66	42	S44 and (normal near2 mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S67	6	**S65 and S66**	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

10/037894 **Chiang Jer Liang**

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Results of search set S115

Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20040250150 A1	Devices, systems and methods for mode driven stops notice	20041209	713/330	
US 20040083072 A1	Controlling the timing of test modes in a multiple processor system	20040429	702/117	
US 20040073780 A1	Single-step processing and selecting debugging modes	20040415	712/227	

US 20040025145 A1	Dynamic software code instrumentation method and system	20040205	717/129
US 20030204707 A1	Real-time tracing microprocessor unit and operating method	20031030	712/227
US 20030204374 A1	Dynamic software code instrumentation method and system	20031030	702/186
US 20030200425 A1	Devices, systems and methods for mode driven stops	20031023	712/229
US 20030114075 A1	Toy vehicle wireless control system	20030619	446/456
US 20030014236 A1	Method and device for assessing performance of micropreocessor execution	20030116	703/26
US 20020133810 A1	Method for hybrid processing of software instructions of an emulated computer system	20020919	717/138
US 20020078329 A1	Watchpoint engine for a pipelined processor	20020620	712/227
US 20020059502 A1	Multicore DSP device having shared program memory with conditional write protection	20020516	711/152
US 20020013918 A1	Devices, systems and methods for mode driven stops	20020131	714/30
US 6839013 B1	Integrated circuit with a high resolution analog to digital convertor, a microcontroller and high de	20050104	341/155
US 6829701 B2	Watchpoint engine for a pipelined processor	20041207	712/227
US 6760866 B2	Process of operating a processor with domains and clocks	20040706	714/34
US 6728901 B1	Arithmetic built-in self-test of multiple scan-based integrated circuits	20040427	714/30
US 6567933 B1	Emulation suspension mode with stop mode extension	20030520	714/31
US 6564339 B1	Emulation suspension mode handling multiple stops and starts	20030513	714/30
US 6557116 B1	Emulation suspension mode with frame controlled resource access	20030429	714/28
US 6553513 B1	Emulation suspend mode with differing response to differing classes of interrupts	20030422	714/28
US 6539497 B2	IC with selectively applied functional and test clocks	20030325	714/30
US 6397382 B1	Dynamic software code instrumentation with cache disabling feature	20020528	717/130
US 6349392 B1	Devices, systems and methods for mode driven stops	20020219	714/30
US 6289300 B1	Integrated circuit with embedded emulator and emulation system for use with such an integrate	20010911	703/28
US 6230119 B1	Integrated circuit with embedded emulator and emulation system for use with such an integrate	20010508	703/27
US 6160734 A	Method for ensuring security of program data in one-time programmable memory	20001212	365/185.04
US 6154760 A	Instruction to normalize redundantly encoded floating point numbers	20001128	708/205
US 6094730 A	Hardware-assisted firmware tracing method and apparatus	20000725	714/28
US 6085336 A	Data processing devices, systems and methods with mode driven stops	20000704	714/30
US 6075937 A	Preprocessing of stored target routines for controlling emulation of incompatible instructions on	20000613	703/23
US 6035422 A	Data processing system for controlling execution of a debug function and method therefor	20000307	714/35
US 6026501 A	Data processing system for controlling execution of a debug function and method thereof	20000215	714/38
US 6009261 A	Preprocessing of stored target routines for emulating incompatible instructions on a target proc	19991228	703/26
US 5974440 A	Microprocessor with circuits, systems, and methods for interrupt handling during virtual task op	19991026	710/262
US 5964893 A	Data processing system for performing a trace function and method therefor	19991012	714/39
US 5900025 A	Processor having a hierarchical control register file and methods for operating the same	19990504	712/248
US 5857094 A	In-circuit emulator for emulating native clustruction execution of a microprocessor	19990105	703/28
US 5832299 A	System for emulating input/output devices utilizing processor with virtual system mode by allow	19981103	710/9
US 5826084 A	Microprocessor with circuits, systems, and methods for selectively bypassing external interrupt:	19981020	718/107
US 5781750 A	Dual-instruction-set architecture CPU with hidden software emulation mode	19980714	712/209
US 5778207 A	Assisting operating-system interrupts using application-based processing	19980707	712/200
US 5752044 A	Computer system having multi-level suspend timers to suspend from operation in attended anc	19980512	713/323
US 5737516 A	Data processing system for performing a debug function and method therefor	19980407	714/38
US 5704034 A	Method and circuit for initializing a data processing system	19971230	714/38
US 5689715 A	Low power ring detect for computer system wake-up	19971118	713/310

US 5644755 A	Processor with virtual system mode	19970701 703/23
US 5644703 A	Data processor providing fast break in program execution	19970701 714/35
US 5630102 A	In-circuit-emulation event management system	19970513 703/28
US 5630078 A	Personal computer with processor reset control	19970513 710/309
US 5623686 A	Non-volatile memory control and data loading architecture for multiple chip processor	19970422 712/32
US 5613144 A	Serial register multi-input multiplexing architecture for multiple chip processor	19970318 712/43
US 5606710 A	Multiple chip package processor having feed through paths on one die	19970225 712/38
US 5598573 A	Multiple chip processor architecture with reset intercept circuit	19970128 711/111
US 5594890 A	Emulation system for emulating CPU core, CPU core with provision for emulation and ASIC ha	19970114 703/23
US 5586302 A	Personal computer system having storage controller with memory write control	19961217 711/154
US 5581779 A	Multiple chip processor architecture with memory interface control register for in-system progra	19961203 712/43
US 5574927 A	RISC architecture computer configured for emulation of the instruction set of a target computer	19961112 712/41
US 5574894 A	Integrated circuit data processor which provides external sensibility of internal signals during re:	19961112 713/500
US 5566344 A	In-system programming architecture for a multiple chip processor	19961015 712/37
US 5560036 A	Data processing having incircuit emulation function	19960924 712/227
US 5548794 A	Data processor and method for providing show cycles on a fast multiplexed bus	19960820 710/51
US 5530804 A	Superscalar processor with plural pipelined execution units each unit selectively having both noi	19960625 714/30
US 5524267 A	Digital I/O bus controller circuit with auto-incrementing, auto-decrementing and non-incrementir	19960604 710/3
US 5493723 A	Processor with in-system emulation circuitry which uses the same group of terminals to output	19960220 703/28
US 5493659 A	Data processor providing fast break in program execution	19960220 712/244
US 5448717 A	Transparently inserting wait states into memory accesses when microprocessor in performing i	19950905 713/600
US 5390332 A	Method and apparatus for performing a takeover of a microprocessor	19950214 710/269
US 5325464 A	Pyramid learning architecture neurocomputer	19940628 706/41
US 5287476 A	Personal computer system with storage controller controlling data transfer	19940215 710/4
US 5274831 A	Microprocessor in response to an interrupt request for executing a microinstruction for samplin	19931228 712/244
US 5249266 A	Data processing apparatus with self-emulation capability	19930928 345/501
US 5185736 A	Synchronous optical transmission system	19930209 370/358
US 5140687 A	Data processing apparatus with self-emulation capability	19920818 703/23
US 5101498 A	Pin selectable multi-mode processor	19920331 710/316
US 5097413 A	Abort circuitry for microprocessor	19920317 714/24
US 5062034 A	Device for emulating a microcontroller using a parent bond-out microcontroller and a derivative	19911029 703/23
US 4998197 A	Data processor with fast break in program execution by selectively processing either external c	19910305 712/227
US 4939637 A	Circuitry for producing emulation mode in single chip microcomputer	19900703 703/26
US 4924382 A	Debugging microprocessor capable of switching between emulation and monitor without acces	19900508 717/134
US 4876639 A	Method and circuitry for causing sixteen bit microprocessor to execute eight bit op codes to pro	19891024 703/27
US 4797808 A	Microcomputer with self-test of macrocode	19890110 714/30
US 4739475 A	Topography for sixteen bit CMOS microprocessor with eight bit emulation and abort capability	19880419 716/19
US 4580216 A	Microcomputer with internal selection of on-chip or off-chip access	19860401 712/37
US 4547849 A	Interface between a microprocessor and a coprocessor	19851015 710/3
US 4459660 A	Microcomputer with automatic refresh of on-chip dynamic RAM transparent to CPU	19840710 711/1
US 4450521 A	Digital processor or microcomputer using peripheral control circuitry to provide multiple memor	19840522 710/3
US 4447874 A	Apparatus and method for communication of information between processes in an information	19840508 719/314
US 4441154 A	Self-emulator microcomputer	19840403 712/43

US 4435763 A	Multiprogrammable input/output circuitry	19840306	703/27
US 4434465 A	Shared microinstruction states in control ROM addressing for a microcoded single chip microc	19840228	712/245
US 4432052 A	Microcomputer device using dispatch addressing of control ROM	19840214	712/245
US 4432051 A	Process execution time accounting system	19840214	717/127
US 4428047 A	Addressing a control ROM in a microcoded single-chip microcomputer using the output signals	19840124	712/230
US 4395757 A	Process synchronization utilizing semaphores	19830726	718/104
US 4394725 A	Apparatus and method for transferring information units between processes in a multiprocessir	19830719	718/106
US 4374409 A	Method of and system using P and V instructions on semaphores for transferring data among	19830215	718/106
US 4369494 A	Apparatus and method for providing synchronization between processes and events occurring	19830118	713/400
US 4351024 A	Switch system base mechanism	19820921	719/310
US 4320451 A	Extended semaphore architecture	19820316	718/106
US 4318182 A	Deadlock detection and prevention mechanism for a computer system	19820302	718/105
US 4316245 A	Apparatus and method for semaphore initialization in a multiprocessing computer system for pı	19820216	718/106
US 4297743 A	Call and stack mechanism for procedures executing in different rings	19811027	718/106
US 4130867 A	Database instruction apparatus for determining a database record type	19781219	707/1
US 4084228 A	Process management structures and hardware/firmware control	19780411	718/103
US 4084224 A	System of controlling procedure execution using process control blocks	19780411	718/100
US 4077058 A	Method and apparatus for executing an extended decor instruction	19780228	717/162
US 4044334 A	Database instruction unload	19770823	707/102
US 4042912 A	Database set condition test instruction	19770816	707/1
US 4025901 A	Database instruction find owner	19770524	707/3
US 4024508 A	Database instruction find serial	19770517	707/1
US 3891974 A	Data processing system having emulation capability for providing wait state simulation function	19750624	703/23
US 20030014236 A	Microprocessor performance determination method involves evaluating performance of microp	20030116	